

I CLAIM:

1. An electronic memory device comprising two or more layers of memory circuitry, each layer comprising circuitry for storing and retrieving information and decoding circuitry for addressing specific information within said information storage circuitry, and where said two or more layers are interconnected by conductors upon which are applied electrical signals that act as the control inputs to said decoding circuitry for addressing specific information.
2. The memory device of claim 1 comprising conductors interconnecting the said two or more layers for carrying the information stored within the device.
3. The memory device of claim 1 wherein only a subset of the said applied electrical signals that act as the control inputs to said decoding circuitry for addressing specific information are applied to the decoding circuitry for addressing specific information of any given layer.
4. The memory device of claim 1 wherein each layer of memory circuitry comprises:
 - a first plurality of generally parallel conductive means;
 - a second plurality of generally parallel conductive means overlapping and generally orthogonal to said first plurality;
 - a non-linear conductive means interconnecting said first and second pluralities of generally parallel conductive means at roughly the points of overlap;
 - decoding means for causing a first voltage on one of the conductive means of the first plurality to differ from the voltages of the remaining conductive means of the first plurality;
 - decoding means for causing a second voltage on one of the conductive means of the second plurality to differ from the voltages of the remaining conductive means of the second plurality;
 - a voltage differential between said first and second voltages sufficient to forward bias a non-linear conductive means at any said point of overlap;
 - a voltage differential between said voltages of the remaining conductive means of the first plurality and said voltages of the remaining conductive means of the second plurality that is not sufficient to forward bias a non-linear conductive means at any said point of overlap.
5. The memory device of claim 4 wherein said non-linear conductive means are absent at some of the points of overlap.
6. An electronic array circuit comprising:
 - a plurality of generally parallel rows and a plurality of generally parallel columns that are generally orthogonal and overlapping;

test circuitry comprising connections between the alternate ends of every evenly numbered row such that continuity of half of the rows can be tested by passing a current;

test circuitry further comprising connections between the alternate ends of every oddly numbered row such that continuity of the other half of the rows can be tested by passing a current.

7. The array circuit of claim 6 comprising:
test circuitry comprising connections between the alternate ends of every evenly numbered column such that continuity of half of the columns can be tested by passing a current;
test circuitry further comprising connections between the alternate ends of every oddly numbered column such that continuity of the other half of the columns can be tested by passing a current.
8. The array circuit of claim 6 comprising testing means for detecting a short-circuit between the evenly numbered rows and the oddly numbered rows.
9. The array circuit of claim 7 comprising testing means for detecting a short-circuit between the evenly numbered columns and the oddly numbered columns.
10. The array circuit of claim 7 comprising testing means for detecting a short-circuit between the rows and the columns.
11. The array circuit of claim 6 wherein ~~the~~ each row exists on a different layer of a multilayered, three-dimensional array.